**REMARKS**

The claims are claims 1 to 5 and 9 to 11.

Claims 1 and 9 are amended. Claims 6 to 8 are canceled. New claims 10 and 11 are added. Claim 1 is amended to correct the problems with antecedent basis pointed out by the Examiner and to distinguish over the rejection. Claim 9 is amended to correspond to amended claim 1. New claims 10 and 11 recite the two alternatives for determining when a burst transfer is complete as taught in the original application at page 12, lines 9 to 24.

Claims 1 to 9 were rejected under 35 U.S.C. 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner pointed out two instances of improper antecedence in claim 1.

Claim 1 has been amended in the manner suggested by the Examiner. Claim 1 as amended is proper under 35 U.S.C. 112.

Claims 1, 2 and 5 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Spasov, Microcontroller Technology: The 68HC11 and Bolt et al U.S. Patent No. 4,769,769. The OFFICE ACTION states that Bolt teaches inhibiting triggering any further transfers until a current transfer is complete at column 2, lines 36 to 40.

Claim 1 recites subject matter not made obvious by the combination of Spasov and Bolt et al. Claim 1 recites "inhibiting the FIFO device from changing state of the FIFO output signal thereby inhibiting of triggering of any further burst transfers until a current burst transfer is complete." This FIFO output signal is the same signal as recited in the previous paragraph that triggers a burst transfer. The OFFICE ACTION cites column 2, lines 36 to 40 of Bolt et al as making obvious the previous limitation. This portion of Bolt et al teaches a "busy/not busy" signal which

inhibits triggering a burst transfer when busy. This is a different signal than the "empty/not empty" signal disclosed in Bolt and also different from the trigger level signal disclosed in Spasov. As taught in this application at page 5, lines 25 to 28 normal practice to avoid interrupting a pending burst transfer is for the DMA unit in the processor to "ignore events requesting service during a current frame transfer." In this invention as recited in claim 1, this interrupting a pending burst transfer is avoiding by the FIFO device inhibiting the change of state signal that triggers a burst transfer. Bolt et al fails to teach that the "empty/not empty" signal is inhibited from changing during a burst transfer as recited in claim 1. Accordingly, claim 1 is allowable over the combination of Spasov and Bolt et al.

Claim 9 recites subject matter not made obvious by the combination of Spasov, Bolt et al and Applicants' Admitted Prior Art. Claim 9 recites "further inhibiting the FIFO device from changing state of the FIFO output signal until a predetermined number of clock cycles following completion of current burst transfer." The OFFICE ACTION cites Applicants' Admitted Prior Art at page 6, lines 6 to 11 as making obvious this subject matter. This portion of the application states:

> "In an example of a direct memory access unit controlled solution, after a frame is completed, the direct memory access unit waits an additional n-clock cycles before checking to determine if the flag is still active."

The phrase "checking to determine if the flag is still active" implies that this flag may be active during that interval of an additional n-clock cycles. This admitted prior art teaches that the DMA of the processor is insensitive to the signal during the additional n-clock cycles. In contrast, the above quoted language of claim 9 recites that this flag (changing state of the FIFO

output signal) cannot be active during this time. Thus claim 9 recites this signal by the FIFO unit cannot be active during the additional n-clock cycles. Thus claim 9 recites a different limitation than that of Applicants' Admitted Prior Art. Accordingly, claim 9 is allowable over the combination of Spasov, Bolt et al and Applicants' Admitted Prior Art.

New claims 10 and 11 recite subject matter not made obvious by the cited art. New claim 10 recites an end of burst signal. No art cited by the Examiner teaches such a signal. New claim 11 recites counting a predetermined number of cycles corresponding to the burst transfer size and "inhibiting the FIFO device from changing state of the FIFO output signal until completion of counting the predetermined number of cycles." No art cited by the Examiner inhibits the change of state signal for such a counted interval.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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